UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,749	06/12/2001	Andrew M. Draper	015114-053600US	5820

26059 7590 12/16/2004

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,749	DRAPER, ANDREW M.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a Final Office Action in response to Amendment filed July 30, 2004. Claims 1-29 are pending and are presently under examination.

2. Prior Office Action rejection for Claims 1, 11, 21 and 28 under 35 U.S.C. 112, second paragraph, with respect to the structural limitation "*programmable logic portion*" for lacking structural cooperative relationship, is hereby withdrawn, in view of the amendment to the claims.

3. Prior art Rejections for Claims 1-29 over Au et al. (US 6681359) is hereby withdrawn, in view of the present Application claiming priority to a US Provisional Application 60/211,094, filed June 12, 2000, which has an earlier filing date than the filing date of the applied reference by Au et al. (US 6681359), filed August 87, 2000.

Drawings

4. The drawings are objected to because this application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klapproth et al. (US 5590354), ISSUED: December 31, 1996.

Regarding independent Claim 1, Klapproth substantially discloses a microcontroller provided with hardware for supporting debugging in compliance with JTAG boundary scans, comprising:

A programmable logic portion (event trace memory, 40), Figure 1.

A first JTAG circuit (JTAG interface, 30), Figure 1, coupled to the programmable logic portion trough interconnection 36, wherein the first JTAG circuit (JTAG interface, 30) comprising a TAP controller (90), Figure 3, coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers DMA_DATA registers (96, 98).

An embedded logic portion (microcontroller 20) comprising a processor (CPU 60) and a second JTAG circuit (JTAG interface, 46), Figure 1, coupled to the first JTAG circuit (JTAG interface, 30) through JTAG connector 28, and to the processor (CPU 60) through DSU 56. The second JTAG circuit (JTAG interface, 46), comprising a TAP controller identical to (90), Figure 3, coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers DMA_DATA registers (96, 98).

Klapproth does not explicitly disclose a first and a second JTAG circuit coupled to a processor located on an integrated circuit, IC. However, Klapproth discloses a (JTAG interface, 30), Figure 1, on a host workstation 32 and a (JTAG interface, 46) with a processor (CPU 60) embedded in a (microcontroller 20) on a PCB board 24.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate JTAG circuits (JTAG interface, 30 and 46) and the processor, in the device of Klapproth, for the purpose of packaging all the discrete parts in the integrated (microcontroller 20). A person skilled in the art would have been motivated to incorporate the discrete parts in an integrated circuit, IC, so as to minimize space, and further to optimize signal integrity by reducing noise interference associated with long interconnections, and thus increasing testing time by avoiding external test equipment.

Regarding Claim 2, Klapproth discloses a first JTAG circuit (JTAG interface, 30) comprising a TAP controller (90), Figure 3, coupled to a first plurality of data registers DMA_DATA registers (96, 98), used for loading data into the programmable logic portion (event trace memory, 40), Figure 1.

Regarding Claim 3, Klapproth discloses a first plurality of data registers DMA_DATA registers (96, 98), comprising a data register (96) for transmitting and receiving from the programmable logic portion (event trace memory, 40) via interconnection 36.

Regarding Claim 4, Klapproth discloses a second plurality of data registers DMA_DATA registers (96, 98) corresponding to the second JTAG circuit (JTAG

interface, 46), comprising data register (96) for transmitting and receiving between the programmable logic portion (event trace memory, 40) via interconnection 64 and the external host workstation 32.

Regarding Claim 5, Klapproth discloses JTAG debug interface block at the target processor side provides the following internal data registers, DMA_ADDR, DMA_DATA, DMA_CONTROL_STATUS, for debug communication purposes that can be read and written bit-sequentially by the host system.

Regarding Claims 6, 7, Klapproth discloses external host workstation 32, which selects a variable length scan chain that consist of serialized flip-flops using a registered boundary scan standard (JTAG) interface that accesses one or more scan chains inside the microprocessor, see Abstract. The scan chain is synchronized using read data, which is captured under synchronization from system clock in register 98. Under external synchronization, first a control pattern is loaded into a circuit, which pattern may be used as well for addressing the circuit in question, and so provides test initialization, see Summary of the Invention.

Regarding Claim 8, Klapproth discloses a first plurality of data registers DMA_DATA registers (96, 98) of (JTAG interface, 46) and a second plurality of data registers DMA_DATA registers (96, 98) of (JTAG interface, 46), where the two sets of data registers operate independently.

Regarding Claim 9, Klapproth discloses an output multiplexer 108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO.

Regarding Claim 10, Klapproth discloses a JTAG bypass register, which is one bit bypass connection between serial input and serial output, using 11111 BYPASS 1 chain bypass mode.

7. Regarding independent Claim 11, Klapproth substantially discloses a microcontroller provided with hardware for supporting debugging in compliance with JTAG boundary scan, including a programmable logic portion (event trace memory, 40) and an embedded logic portion (microcontroller 20) Figure 1, the embedded logic portion, comprising:

A processor (CPU 60) and a first JTAG circuit (JTAG interface, 46), Figure 1, coupled to the processor (CPU 60) through DSU 56 and a second JTAG circuit (JTAG interface, 30) coupled to the programmable logic portion (event trace memory, 40), Figure 1, trough interconnection 36.

The first JTAG circuit (JTAG interface, 46) comprising a TAP controller identical to (90), Figure 3 coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers DMA_DATA registers (96, 98).

Klapproth does not explicitly disclose an embedded logic portion of an integrated circuit, IC having a programmable logic portion. However, Klapproth discloses a JTAG circuit (JTAG interface, 30), Figure 1, on a host workstation 32, a JTAG circuit (JTAG interface, 46) with a processor (CPU 60) embedded in a (microcontroller 20) and a programmable logic portion (event trace memory, 40) on a PCB board 24.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate the JTAG circuits (JTAG interface, 30 and 46), the processor (CPU 60) and the programmable logic portion (event trace memory, 40) in the device of Klapproth, for the purpose of packaging all the discrete parts in the integrated (microcontroller 20). A person skilled in the art would have been motivated to incorporate the discrete parts in an integrated circuit, IC, so as to minimize space, and further to optimize signal integrity by reducing noise interference associated with long interconnections, and thus increasing testing time by avoiding external test equipment.

Regarding Claims 12, 13, 14, 15, Klapproth discloses a second JTAG circuit (JTAG interface, 30) comprising a TAP controller identical to (90), Figure 3, coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers, further comprising a JTAG bypass register, which is one bit bypass connection between serial input and serial output, using 11111 BYPASS 1 chain bypass mode and a data registers (98, 96) that capture data during CAPTURE_DR. The data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO, and furthermore loading data into the programmable logic portion (event trace memory, 40), Figure 1. The data registers DMA_DATA registers (96, 98), comprising a data register (96), which allows a user to transmit and receive from the programmable logic portion (event trace memory, 40) via interconnection 36.

Regarding Claim 16, Klapproth discloses a second plurality of data registers DMA_DATA registers (96, 98) corresponding to second JTAG circuit (JTAG interface, 46), comprising a data register (96) for transmitting and receiving between the programmable logic portion (event trace memory, 40) via interconnection 64 and the external host workstation 32.

Regarding Claim 17, Klapproth discloses JTAG debug interface block at the target processor side, which provides the following internal data registers, DMA_ADDR, DMA_DATA, DMA_CONTROL_STATUS, for debug communication purposes that can be read and written bit-sequentially by the host system.

Regarding Claim 18, Klapproth discloses an external host workstation 32, which selects a variable length scan chain that consist of serialized flip-flops using a registered boundary scan standard (JTAG) interface that accesses one or more scan chains inside the microprocessor, see Abstract.

Regarding Claim 19, Klapproth discloses an output multiplexer 108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO.

Regarding Claim 20, Klapproth does not explicitly disclose a second multiplexer coupled to an output from the first multiplexer, the first instruction register, and a data output of the second JTAG circuit, where the second multiplexer is controlled by the JTAG circuit. However, Klapproth discloses an identical multiplexer108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO. It would have been obvious

to a person having ordinary skill in the art at the time the invention was made to use the identical multiplexer108, as taught by Klapproth, to select the appropriate JTAG signals. A person skilled in the art would have been motivated to use an identical multiplexer, as a cost effective tool, by avoiding unique switching design.

8. Regarding independent Claim 21, Klapproth substantially discloses a method using a microcontroller provided with hardware for supporting debugging in compliance with JTAG boundary scan, and using a PCB board 24 that comprises a first processor (CPU 60) and a programmable logic portion (event trace memory, 40), the method comprising:

Transmitting first data signals between pins of (probe 38) and circuitry in the programmable logic portion (event trace memory, 40) using a first JTAG circuit (JTAG interface, 30), Figure 1, coupled to the programmable logic portion trough interconnection 36.

Transmitting second data signals between an external (HOST) processor 32 and the first processor (CPU 60) using a second JTAG circuit (JTAG interface, 46) in an embedded logic portion (microcontroller 20).

Klapproth does not explicitly use a chip that comprises a first processor and a programmable logic portion. However, Klapproth uses a PCB board 24 that comprises a first processor (CPU 60) and a programmable logic portion (event trace memory, 40). Furthermore, Klapproth discloses a JTAG circuit (JTAG interface, 30), Figure 1, on a host workstation 32, a JTAG circuit (JTAG interface, 46) with a processor (CPU 60)

embedded in a (microcontroller 20), and a programmable logic portion (event trace memory, 40) on a PCB board 24.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate the JTAG circuits (JTAG interface, 30 and 46), the processor (CPU 60) and the programmable logic portion (event trace memory, 40) in the device of Klapproth, for the purpose of packaging all the discrete parts in the integrated (microcontroller 20). A person skilled in the art would have been motivated to incorporate the discrete parts in an integrated circuit, IC, so as to minimize space, and further to optimize signal integrity by reducing noise interference associated with long interconnections, and thus increasing testing time by avoiding external test equipment.

Regarding Claim 22, Klapproth discloses a first and a second JTAG circuit (JTAG interface, 30 and 46), Figure 1, comprising a TAP controller identical to (90), Figure 3.

Regarding Claim 23, Klapproth discloses first JTAG circuit (JTAG interface, 30) comprising a TAP controller (90), Figure 3, coupled to a first plurality of data registers DMA_DATA registers (96, 98), used for loading data into the programmable logic portion (event trace memory, 40), Figure 1.

Regarding Claim 24, Klapproth discloses a second plurality of data registers DMA_DATA registers (96, 98), second JTAG circuit (JTAG interface, 46), comprising a data register (96) for transmitting and receiving between the programmable logic portion (event trace memory, 40) via interconnection 64 and the external host workstation 32.

Regarding Claim 25, Klapproth discloses an output multiplexer 108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO.

Regarding Claim 26, Klapproth does not explicitly disclose a second multiplexer coupled to an output from the first multiplexer, the first instruction register, and a data output of the second JTAG circuit, where the second multiplexer is controlled by the JTAG circuit. However, Klapproth discloses an identical multiplexer108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the identical multiplexer108, as taught by Klapproth, to select the appropriate JTAG signals. A person skilled in the art would have been motivated to use an identical multiplexer, as a cost effective tool, by avoiding unique switching design.

9. Regarding independent Claim 27, Klapproth substantially discloses a microcontroller provided with hardware for supporting debugging in compliance with JTAG boundary scan, comprising:

A processor (HOST, 32), comprising a first JTAG circuit (JTAG interface, 30), Figure 1. The first JTAG circuit (JTAG interface, 30) comprising a TAP controller identical to (90), Figure 3 coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers DMA_DATA registers (96, 98).

A second JTAG circuit (JTAG interface, 46) coupled to the first JTAG circuit (JTAG interface, 30) via JTAG connector 28. The second JTAG circuit (JTAG interface, 46) comprising a TAP controller identical to (90), Figure 3 coupled to a first instruction register (IR, comprising a parallel load register 102 and a shift register 104), and a plurality of data registers DMA_DATA registers (96, 98). The plurality of data registers of the second JTAG circuit (30) performs data functions that are different than the functions performed by the data registers of the first JTAG circuit (46).

Klapproth does not explicitly disclose an embedded logic portion of an integrated circuit, IC having a programmable logic portion. However, Klapproth discloses a JTAG circuit (JTAG interface, 30), Figure 1, on a host workstation 32, a JTAG circuit (JTAG interface, 46) with a processor (CPU 60) embedded in a (microcontroller 20) and a programmable logic portion (event trace memory, 40) on a PCB board 24.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate the JTAG circuits (JTAG interface, 30 and 46), the second JTAG circuit, the processor (CPU 60) and the programmable logic portion (event trace memory, 40) in the device of Klapproth, for the purpose of packaging all the discrete parts in the integrated (microcontroller 20). A person skilled in the art would have been motivated to incorporate the discrete parts in an integrated circuit, IC, so as to minimize space, and further to optimize signal integrity by reducing noise interference associated with long interconnections, and thus increasing testing time by avoiding external test equipment.

Regarding Claim 28, Klapproth discloses an embedded logic portion (microcontroller 20) and a programmable logic portion (event trace memory, 40) coupled to the first JTAG circuit (JTAG interface, 30), via interconnect 36, Figure 1. The second JTAG circuit (JTAG interface, 46) is part of the embedded logic portion (microcontroller 20).

Regarding Claim 29, Klapproth discloses an output multiplexer 108 that feeds result data output line TDO. At CAPTURE_DR the data is transferred from register 98 to register 96 and serial out via multiplexer 108 and TDO.

Response to Arguments

10. Applicant's arguments, see REMARKS/ ARGUMUNTS on page 8 and 9 of the AMENDMENT, filed July 30, 2004, with respect to the rejections of claim 27 under 35 U.S.C. 102(e) as being anticipated by Au et al. (US 6681359), and claims 1-26, 28 and 29 under 35 U.S.C. 103(a) as being unpatentable over Au et al. (US 6681359) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of claims 1-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Klapproth et al. (US 5590354), as set forth in the preset Office Action.

Applicant's arguments with respect to the prior art rejection by Au et al. (US 6681359) with respect to claims 1-29 have been considered but are moot in view of the new grounds of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (571) 273-3824
Email: james.kerveros@uspto.gov

Date: 1 December 2004
Office Action: Final Rejection

By: _____ 12/1/04

JAMES C KERVEROS
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100